Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A packet processing unit ~~for outputting a packet to a transmission channel after performing destination address on said packet received from said transmission channel~~, comprising:

packet receiving means for outputting ~~the~~ a packet received via ~~said~~ a first transmission channel in the form of split cells of a fixed length,

search key extracting means for extracting a predetermined search key from said cells ~~received~~ output from said packet receiving means,

a CAM for performing retrieval of a memory address based on said search key extracted ~~in~~ by said search key extracting means and for outputting said memory address, ~~corresponding to said key~~

associative data storing means for storing at least destination information and for outputting ~~the~~ information stored ~~in the~~ at an input memory address,

associative data reading means for calculating ~~the~~ a particular memory address of said associative data storing means based on said memory address ~~received~~ output from said CAM and for supplying the particular memory address to said associative data storing means,

destination address means for ~~performing~~ updating a destination address of a particular cell of said cells based on ~~the~~ particular information ~~of~~ output from said associative data storing means that is stored at said particular memory address in said associative data storing means ~~read by said associative data reading means~~ and for outputting said cells, and

packet transmitting means for ~~putting~~ combining the cells ~~received~~ output from said destination address means ~~back to a~~ into an updated packet and for outputting said updated packet to ~~said~~ a second transmission channel,

wherein said packet receiving means, said search key extracting means, said CAM, ~~associative data storing means,~~ said associative data reading means, said associative data storing means, said destination address means, and said packet transmitting means are configured to perform ~~a pipeline~~ processing as stages of a pipeline.

2. (Currently Amended) ~~A~~ The packet processing unit as claimed in claim 1, wherein a duration of each stage of said stages of said pipeline ~~said packet receiving means, search key extracting means, CAM, associative data storing means, associative data reading means, destination address means and packet transmitting means are~~ is set at not more than an arriving time interval ~~of the packet input in~~ at which packets are received by said packet receiving means.

3. (Currently Amended) ~~A~~ The packet processing unit as claimed in claim 2, wherein a processing time of each of said packet receiving means, said search key extracting means, said CAM, said associative data storing means, said associative data reading means, said destination address means, and said packet transmitting means ~~are~~ is set at not more than the duration of each stage of said stages of said pipeline.

4. (Currently Amended) ~~A~~ The packet processing unit as claimed in claim ~~3~~ 1, further comprising:

maintenance means for performing maintenance of at least one of said CAM during an idle time of said CAM or said associative data storing means during an idle time of said ~~stage~~ associative data storing means.

5. (Currently Amended) ~~A~~ The packet processing unit as claimed in claim 1, further comprising:

buffer means for providing a timing adjustment between said first transmission channel and said packet receiving means and between said second transmission channel and said packet transmitting means.

6. (Currently Amended) ~~A~~ The packet processing unit as claimed in claim 1, further comprising:

arithmetic processing means for performing a predetermined process with respect to said cells ~~in~~ as at least one of a following step to said packet receiving means or a preceding step to said packet transmitting means.

7. (Currently Amended) ~~A~~ The packet processing unit as claimed in claim 2, further comprising:

buffer means for providing a timing adjustment between said first transmission channel and said packet receiving means and between said second transmission channel and said packet transmitting means.

8. (Currently Amended) ~~A~~ The packet processing unit as claimed in claim 3, further comprising:

buffer means for providing a timing adjustment between said first transmission channel and said packet receiving means and between said second transmission channel and said packet transmitting means.

9. (Currently Amended) ~~A~~ The packet processing unit as claimed in claim 4, further comprising:

buffer means for providing a timing adjustment between said first transmission channel and said packet receiving means and between said second transmission channel and said packet transmitting means.

10. (Currently Amended) ~~A~~ The packet processing unit as claimed in claim 2, further comprising:

arithmetic processing means for performing a predetermined process with respect to said cells ~~in~~ as at least one of a following step to said packet receiving means or a preceding step to said packet transmitting means.

11. (Currently Amended) ~~A~~ The packet processing unit as claimed in claim 3, further comprising:

arithmetic processing means for performing a predetermined process with respect to said cells ~~in~~ as at least one of a following step to said packet receiving means or a preceding step to said packet transmitting means.

12. (Currently Amended) ~~A~~ The packet processing unit as claimed in claim 4, further comprising:

arithmetic processing means for performing a predetermined process with respect to said cells ~~in~~ as at least one of a following step to said packet receiving means or a preceding step to said packet transmitting means.

13. (Currently Amended) ~~A~~ The packet processing unit as claimed in claim 5, further comprising:

arithmetic processing means for performing a predetermined process with respect to said cells ~~in~~ as at least one of a following step to said packet receiving means or a preceding step to said packet transmitting means.

14. (New) The packet processing unit as claimed in claim 1,

wherein said second transmission channel is a same transmission channel as said first transmission channel.

15. (New) A packet processing unit, comprising:

a packet receiving circuit for receiving a packet over a first transmission channel, and for splitting said packet into a plurality of cells while receiving said packet, and for outputting said plurality of cells, each cell of said plurality of cells having a fixed length;

a search key extracting circuit for extracting one or more search keys from a first cell of said plurality of cells output by said packet receiving circuit and for outputting said one or more search keys;

a content addressable memory for retrieving one or more memory addresses based on said one or more search keys output by said search key extracting circuit, and for outputting said one or more memory addresses;

a matching entry address receiving and associative data address transmitting circuit for calculating one or more particular memory addresses based on said one or more memory addresses output by said content addressable memory, and for outputting said one or more particular memory addresses;

an associative data memory for outputting one or more associative data results that are read from said associative data memory at said one or more particular memory addresses that are output by said matching entry address receiving and associative data address transmitting circuit;

a search result receiving circuit for modifying said first cell of said plurality of cells based on at least one of said one or more associative data results output by said associative data memory, and for outputting said plurality of cells after modifying said first cell; and

a packet transmitting circuit for combining said plurality of cells output from said search result receiving circuit into a modified packet, and for outputting said modified packet over a second transmission channel.

16. (New) The packet processing unit of claim 15,

wherein said second transmission channel is a same transmission channel as said first transmission channel.

17. (New) The packet processing unit of claim 15,

wherein each cell of said plurality of cells passes through each of said packet receiving circuit, said search key extracting circuit, said content addressable memory, said matching entry address receiving and associative data address transmitting circuit, said associative data memory, said search result receiving circuit, and said packet transmitting circuit.

18. (New) The packet processing unit of claim 15,

wherein said packet receiving circuit, said search key extracting circuit, said content addressable memory, said matching entry address receiving and associative data address transmitting circuit, said associative data memory, said search result receiving circuit, and said packet transmitting circuit are configured to perform processing as stages of a pipeline.

19. (New) The packet processing unit of claim 18,

wherein each stage of said pipeline is configured to perform processing for each cell of said plurality of cells in a predetermined amount of time; and

wherein said search key extracting circuit is configured to extract two or more search keys from said first cell during said predetermined amount of time and is configured to output said two or more search keys; and

wherein said content addressable memory is configured to retrieve two or more memory addresses based on said two or more search keys during said predetermined amount of time, and is configured to output said two or more memory addresses.

20. (New) The packet processing unit of claim 18,

wherein a time between said packet receiving circuit receiving said packet and said packet transmitting circuit outputting said modified packet is less than a time interval between arrival of packets to said packet receiving circuit; and

wherein said content addressable memory is configured to allow for updating during an idle time when no processing is being performed by said content addressable memory.